IN THE SPECIFICATION:

Please insert a new paragraph and section heading directly preceding the first paragraph and section heading on page 3 as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application Serial No. 08/833,974, filed April 11, 1997, now U.S. Patent 6,066,539 issued May 23, 2000.

Please amend the paragraph bridging pages 2 and 3 as follows:

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. The advantages of increased miniaturization of components include: ~~reduced bulk~~ reduced-bulk electronic equipment, improved reliability by reducing the number of solder or plug connections, lower assembly and packaging costs, and improved circuit performance. In pursuit of increased miniaturization, DRAM chips have been continually redesigned to achieved ever-higher degrees of integration which has reduced the size of the DRAM. However, as the dimensions of the DRAM are reduced, the occupied area of each unit memory cell of the DRAM must be reduced. This reduction in occupied area necessarily results in a reduction of the dimensions of the capacitor, which, in turn, makes it difficult to ensure required storage capacitance for transmitting a desired signal without malfunction. However, the ability to densely pack the unit memory cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of DRAM devices are to be successfully manufactured.

Please amend the third full paragraph on page 6 as follows:

FIG. 23 is an illustration of a scanning electron micrograph of a side ~~cross-sectional~~ cross-sectional view of a storage poly after etching in the formation of a capacitor according to the present invention;

Please amend the paragraph bridging pages 7 and 8 as follows:

A mask layer 124, preferably silicon dioxide with a thickness of about 350 angstroms, is deposited over the HSG polysilicon layer 122, as shown in FIG. 3. An upper portion of the mask layer 124 is then removed, preferably facet etched (dry etching, sputter etching, and planarization may also be used), to form micro openings 126 to expose the uppermost portions ~~126 of~~ of the HSG polysilicon layer 122, as shown in FIG. 4. Preferably, about 50 to 75% of the HSG polysilicon layer 122 will be exposed. As shown in FIG. 5, a photo-resist material 128 is then deposited to pattern a desired position of the memory cell capacitor (the HSG polysilicon layer 122 and the mask layer 124 are shown as a single layer 130).

Please amend the second full paragraph on page 8 as follows:

The exposed uppermost HSG polysilicon layer portions ~~126~~ 122 are then etched by a dry anisotropic etch, with an etchant which is highly selective to the mask layer 124, preferably selective at a ratio of about 70:1 or higher, as shown in progress in FIG. 8. A preferred selective etch chemistry would contain chlorine gas as the primary etchant with passivation for the barrier layer 119 (silicon dioxide) being hydrogen bromide gas (i.e., the hydrogen bromide prevents the etching of the silicon dioxide barrier layer 119 which, in turn, prevents the source region 107 from being etched). Selective etching is the use of particular etchants which etch only a particular material or materials while being substantially inert to other materials.

Please amend the third full paragraph on page 8 as follows:

The etching translates the pattern of the exposed uppermost HSG polysilicon layer portions ~~126~~ 122 into the storage poly 120. Any remaining mask layer material 124 is then removed, preferably by a wet or in situ etch. The etching of the storage poly 120 results in an etched structure 132 having convoluted openings 134, shown with the convoluted openings 134 greatly exaggerated in FIG. 9. Capacitors 136 are completed by depositing a dielectric material

layer 138 over the etched structure 132 and depositing a cell poly layer 140 over the dielectric material layer 138, such as shown in FIG. 10.

Please amend the paragraph bridging pages 9 and 10 as follows:

As shown in FIG. 13, a resist material 146 is patterned on the second barrier layer 144, such that predetermined areas of the memory cell capacitor formation will be etched. The second barrier layer 144 and the first barrier layer 142 are etched to ~~exposed~~ expose a portion of the semiconductor substrate 102, as shown in FIG. 14. The transistor insulating spacer members 113 and the cap insulator 115 each being made of silicon nitride resists the etchant and thus prevents shorting between the word line 112 and the capacitor to be formed. The resist material 146 is then removed, as shown in FIG. 15, and a layer of amorphous silicon 148, which upon subsequent annealing will become polysilicon, is then applied over second barrier layer 144 to make contact with the semiconductor substrate 102, as shown in FIG. 16. The amorphous silicon layer 148 is then planarized down to the second barrier layer 144 to form silicon plugs 150, as shown in FIG 17. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process.

Please amend the paragraph bridging pages 10 and 11 as follows:

A mask layer 124 is deposited over the HSG polysilicon layer 122. The upper portion of the mask layer 124 is then removed to expose the uppermost portions ~~126~~ (micro openings 126) of the HSG polysilicon layer 122, as shown in FIG. 20. The exposed HSG polysilicon layer portions ~~126 are~~ 122 are then etched, as previously shown in FIG. 8. The etching of the silicon plugs 150 results in an etched structure 152 having convoluted openings 154, shown with the convoluted openings 154 greatly exaggerated in FIG. 21. The memory cell capacitors are completed by depositing a dielectric material layer over the etched structure 152 and depositing a cell poly layer over the dielectric material layer, as previously described for FIG. 10.